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1. Field of the Invention The present invention relates to the field of microprocessors and, more particularly, to timing of execution of instructions, especially non-predicated instructions, in microprocessors. 2. Description of the Related Art Almost all personal computer systems utilize a system interrupt mechanism. With respect to microprocessors, such interrupt mechanisms typically take the form of a pending interrupt. Each pending interrupt usually specifies a single event that has occurred. If a processor receives a pending interrupt request while it is currently processing another instruction, the processor temporarily sets aside execution of the instruction being processed and starts execution of the interrupt handler. Execution of the interrupt handler typically takes precedence over execution of the instruction being processed by the microprocessor. Once the interrupt is serviced, if the processor is finished servicing the interrupt, it restarts execution of the instruction being processed, and if the processor is not finished servicing the interrupt, it is again temporarily placed aside for processing of the pending interrupt. This mechanism is not well suited to handling of an event that may be required multiple times during execution of a single program. For example, an interrupt may be required while executing a loop within the program in order to test the data within the loop. Using the prior art interrupt mechanism, if the processor receives an interrupt while it is in the middle of executing the loop, processing of the loop is restarted and the processor immediately resets itself for execution of the interrupt. One alternative to providing a pending interrupt is to use a

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